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MS APPEAL BRIEF - PATENTS
PATENT
1248-0509P

IN THE U.S. PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF		BEFORE THE BOARD OF APPEALS	
Kumi MIYACHI et al.		Appeal No.:	
APPL. NO.:	09/615,956	GROUP:	2133
FILED:	July 13, 2000	EXAMINER:	E. Abraham

For: SEMICONDUCTOR DEVICE HAVING INTEGRALLY SEALED INTEGRATED CIRCUIT CHIPS ARRANGED FOR IMPROVED TESTING

APPEAL BRIEF TRANSMITTAL FORM

MS APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

April 26, 2004

Sir:

Transmitted herewith is an Appeal Brief (in triplicate) on behalf of the Appellants in connection with the above-identified application.

☐ The enclosed document is being transmitted via the Certificate of Mailing provisions of 37 C.F.R. § 1.8.

A Notice of Appeal was filed on February 24, 2004.

05/06/2004 VJONES2 00000001 022448 09615956
01 FC:1402 330.00 DA

☐ Applicant claims small entity status in accordance with 37 C.F.R. § 1.27

The fee has been calculated as shown below:

☐ Extension of time fee pursuant to 37 C.F.R. §§ 1.17 and 1.136(a) - $0.00.

☒ Fee for filing an Appeal Brief - $330.00 (large entity).

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☐ Please charge Deposit Account No. 02-2448 in the amount of $0.00. A triplicate copy of this sheet is attached.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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APPEAL BRIEF ON BEHALF OF APPELLANTS:
Kumi MIYACHI et al.

MS Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

April 26, 2004

Sir:

I. REAL PARTY IN INTEREST

The real party in interest for this application is the Assignee, SHARP KABUSHIKI KAISHA, of 22-22 Nagaike-cho, Abeno-ku, Osaka 545-8522, Japan.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences pending with respect to the subject matter of the present application.

III. STATUS OF CLAIMS

Claims 2-4, 6, 7, 9, 10, 11, and 13-16 remain pending, claims 1, 5, 8, and 12 having previously been cancelled. Claims 2, 3, 6, 7, 9, 10, 13 and 14 are independent. No claims have been allowed.

IV. STATUS OF AMENDMENTS

An amendment was filed January 26, 2004 that included an amendment to clarify language in claim 13. That amendment was not entered by the Examiner (as verified by a telephone conversation with the Examiner on March 25, 2004). Instead an Advisory Action was issued February 9, 2004.

V. SUMMARY OF THE INVENTION

The present invention is directed to an integrally sealed semiconductor device suitable for performing boundary scan testing thereon. The present invention provides specific connection arrangements between plural chips contained in the integrally sealed semiconductor device such that it obtains a smaller size than a conventional "stacked package". A set of embodiments has been disclosed having specific connection structure between chips, and are disclosed as progressively reduced sized packages.

The present invention, in a preferred embodiment (see **Figures 3 and 4**), is directed to a semiconductor device comprising a plurality of chips, which are integrally sealed air-tight (e.g., see Figures 2 and 4). In this preferred embodiment, the chips can be arranged in a dual-in-line package and in order to accomplish a connection between chips, each chip is connected to each

other through an output pin of the semiconductor device. By not having direct connections between chips, the size of the semiconductor device can be further reduced. The semiconductor device thus comprises a test signal input terminal (e.g., Figures 1 and 3, pin BI); a test result output terminal for outputting a test result of the plurality of chips to outside (e.g., Figures 1 and 3, pin BO); and control signal input terminals (e.g., Figures 1 and 3, pins BC, BM, and BR). The test signal inputted from the test signal input terminal is successively transferred through the plurality of chips (e.g., Figure 3, wire WO and WOI connecting signal line TDO to TDI), and the test control signals inputted from the control signal input terminals are individually supplied to each of the plurality of chips (e.g., Figure 3, signal lines TCK, TMS, TRST connected, parallel to each other, via wires WC, WM, and WR). Further, as can be seen in Figure 4, chips can be arranged in a dual in line (DIL) structure, being mounted on front and back surfaces of a substrate 32, and connected to each other via test commands/data output pin BO (specification at paragraph bridging pages 17 and 18).

The present invention, in an alternative preferred embodiment (see **Figure 5**), is directed to a semiconductor device comprising a plurality of chips, which are integrally sealed air-tight (e.g., Figures 2, 4). In this preferred embodiment the connection structure is such that only one of a plurality of chips contains the required test circuit, thus enabling a further reduction in the size of the package. The semiconductor device in this embodiment thus

comprises a test signal input terminal (e.g., pin BI); a test result output terminal (e.g., pin B0); control signal input terminals (e.g., pins BC, BM, and BR), only one of the plurality of chips being connected to the test signal input terminal, to the test result output terminal, and to the control signal input terminals (e.g. Figure 5, where the one chip ic1a is connected to wires WI, W0, WC, WM, and WR; specification, page 20, lines 19-23), the test signal being inputted to the one of said plurality of chips and successively transferred through the other chips, and after being inputted again into the one of said plurality of chips, outputted as the test result outside (e.g., Figure 5, connections via wires W0I and W0), the test control signals being individually supplied from the one of the plurality of chips to each of the other chips (e.g., Figure 5, connections via wires W10, W11, W12).

The present invention, in still a further preferred embodiment (see **Figures 3, 4, and 6**), is directed to a semiconductor device in which a plurality of chips are integrally sealed air-tight (e.g., Figure 4). In this embodiment, further reduction in size can also be obtained by sealing connecting wires within the integrally sealed package and by eliminating pins in the chips. Instead connection to the chips is by way of pads. The semiconductor device comprising a test register provided between a core logic and each of input and output terminals of each chip (e.g., Figure 6, boundary scan register 2); and a control circuit for controlling the test register (e.g., TAPC 7), a test commands/data input pin of a device (e.g., Figure 3, TDI of device 31) is

connected to the test commands/data input pad of a chip of a first stage (e.g., Figure 3, TDI of ic1), and the test commands/data output pad of a chip (e.g., Figure 3, TDO of ic1) is connected to a corresponding output pin of the device (e.g., Figure 3, TDO of device 31) and serially to the test commands/data input pad of a chip of a following stage via the output pin of the device (e.g., Figure 3, TDI of ic2 via wire WOI), and input pins of the device for the signals to be used in the test (e.g., Figure 3, TCK, TMS, and TRST via wires WC, WM, and WR) is connected to the corresponding input pins of the signals of each chip, connection being performed via wires sealed with the plurality of chips.

The present invention, in still another preferred embodiment (see **Figures 5, and 6**), is directed to a semiconductor device in which a plurality of chips are integrally sealed air-tight. In this embodiment, reduction in package size is achieved by way of a loop connection structure that enables only one chip having to contain the test logic, elimination of pins in the chips, and including wires in the integrally sealed package. The semiconductor device comprising a test register provided between a core logic and each of input and output terminals of each chip (e.g., Figure 6, boundary scan register 2); and a control circuit for controlling the test register for testing the chip (e.g., TAPC 7), test commands/data input and output pins of a device (e.g., Figure 5, TDI and TDO of the device 41) is respectively connected to the test commands/data input and output pads of the chip of the first stage (e.g., Figure 5, TDI and TD0a of ic1a, respectively), and the relay output pad of the chip of the first stage (e.g.,

Figure 5, TDO of ic1a) is connected to a test commands/data input pad of a chip of a following stage (e.g., Figure 5, TDI of ic2a), and a test commands/data output pad (e.g., Figure 5, TD0 of ic2a) and a test commands/data input pad (e.g., Figure 5, TDI of ic3a) is serially and successively connected between chips of a preceding stage and a following stage, and a test commands/data output pad of a chip of a last stage (e.g., Figure 5, TDO of ic3a) is connected to the relay input pad of the chip of the first stage (e.g., Figure 5, TDIa of ic1a) so as to form a loop, and the output pads of the chip of the first stage for the signals to be used in the test (e.g., Figure 5, TAP0 to TAP4 of ic1a) is connected to input pads of the signals of the other chips (e.g., Figure 5, TAP0 to TAP4 of ic2a and 1c3a, respectively), connection being performed via wires sealed with the plurality of chips.

An still further, the present invention is directed to a semiconductor device (see **Figures 2 and 4**) wherein the plurality of chips are stacked.

VI. THE GROUNDS OF REJECTION

The Examiner has rejected all pending claims as follows:

Claims 2-4, 6, 7, 9-11, and 13-16 stand rejected under 35 U.S.C. 103(a) as being unpatentable over *Brown et al.* (U.S. Patent No. 5,627,842, hereinafter "Brown"), in view of *Fehr et al.* (U.S. Patent No. 6,058,602, hereinafter "Fehr").

VII. ISSUES ON APPEAL

The issues to be resolved in this appeal are whether claims 2-4, 6, 7, 9-11 and 13-16 are unpatentable under 35 U.S.C. 103(a) based on the teachings of Brown and Fehr.

VIII. GROUPING OF CLAIMS

The claims should be grouped as follows for purposes of this Appeal:

(1) Claim 4 is separately grouped and argued;

(2) Claim 11 is separately grouped and argued;

(3) Claim 14 is separately grouped and argued;

(4) Claim 13 is separately grouped and argued;

(5) Claims 3, 7, and 10 stand or fall together;

(6) Claims 2, 6, and 9 stand or fall together;

(7) Claim 15 is separately grouped and argued; and

(8) Claim 16 is separately grouped and argued.

IX. ARGUMENT

A. Rejection of claim 4 under 35 U.S.C. 103(a)

1. Argument Summary

The reasoning provided in support of the rejection of claim 4 under 35 U.S.C. § 103(a) as being unpatentable over *Brown* and *Fehr* fails to establish *prima facie* obviousness. Generally, the deficiency of the rejection is that even if it can be said that the combination Brown and Fehr teach the invention of

claim 3, which Appellants do not admit, the combination fails to show or suggest at least the additional feature recited in claim 4.

2. The Legal Requirements of *Prima Facie* Obviousness

To establish *prima facie* obviousness, all claim limitations must be taught or suggested by the prior art and the asserted modification or combination of the prior art must be supported by some teaching, suggestion, or motivation in the applied references or in knowledge generally available to one skilled in the art. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). The prior art must suggest the desirability of the modification in order to establish a *prima facie* case of obviousness. In re Brouwer, 77 F.3d 422, 425, 37 USPQ2d 1663, 1666 (Fed. Cir. 1995). It can also be said that the prior art must collectively suggest or point to the claimed invention to support a finding of obviousness. In re Hedges, 783 F.2d 1038, 1041, 228 USPQ 685, 687 (Fed. Cir. 1986); In re Ehrreich, 590 F.2d 902, 908-909, 200 USPQ 504, 510 (C.C.P.A. 1979).

Furthermore, when considering the differences between the primary reference and the claimed invention, the question for assessing obviousness is not whether the differences themselves would be been obvious, but instead whether the claimed invention as a whole would have been obvious. Stratoflex Inc. v. Aeroquip Corp., 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983).

3. The rejection fails to establish *prima facie* obviousness of claim 4

Claim 4 is directed to the invention of claim 3, as well as, wherein only the one of the plurality of chips includes a controller for controlling an input/output interface of the test signal. Claim 3 recites that, "only one of said plurality of chips being connected to said test signal input terminal, to said test result output terminal, and to said control signal input terminals" and "the test signal being inputted to the one of said plurality of chips and successively transferred through the other chips, and after being inputted again into the one of said plurality of chips, outputted as the test result outside." Thus, the invention of claim 4 is directed to a semiconductor device where only one of a plurality of chips includes the required controller for controlling an input/output interface of the test signal, and the test signal is successively transferred through the other chips (e.g., see Figure 5). By including the controller in only one of the chips, the size of the package is further reduced (Specification at page 21, lines 18-23). The arguments presented herein for claim 3 apply as well to claim 4.

The final Office Action refers back to a previous Office Action of July 31, 2003 (hereinafter "the July 31 Office Action"). With respect to claim 4, the July 31 Office Action states that, "Brown et al. in view of Fehr disclose all subject matter claimed in claim 3 including Brown et al. teach a chip that includes a

controller (TAP controller) for controlling an input/output interface of the test signal (see Fig. 4, "TAP controller").

Appellants agree that Brown teaches "a" chip in the standard-compliant board includes a controller. However, the claim is directed to, among other things, a semiconductor device having a plurality of chips, wherein "only the one of said plurality of chips includes a controller for controlling an input/output interface of the test signal." Thus, Appellants submit that the rejection fails to establish *prima facie* obviousness for claim 4.

B. Rejection of claim 11 under 35 U.S.C. 103(a)

1. Argument Summary

The reasoning provided in support of the rejection of claim 11 under 35 U.S.C. § 103(a) as being unpatentable over *Brown* and *Fehr* fails to establish *prima facie* obviousness. Generally, the deficiency of the rejection is that even if it can be said that the combination Brown and Fehr teach the invention of claim 10, which Appellants do not admit, the combination fails to show or suggest at least the additional feature recited in claim 11.

2. The rejection fails to establish *prima facie* obviousness of claim 11

Claim 11 is directed to the invention of claim 10, as well as, wherein only the one of the plurality of chips includes a controller for controlling an input/output interface of the test signal. Claim 10 recites that, "only one of said plurality of chips being connected to said test signal input pin, to said test

result output pin, and to said control signal input pins" and "the test signal being inputted to the one of said plurality of chips and successively transferred through the other chips so connected to each other by wires sealed with the plurality of chips, and after being inputted again into the one of said plurality of chips, outputted as the test result to outside." Thus, the invention of claim 11 is directed to a semiconductor device where only one of a plurality of chips includes the required controller for controlling an input/output interface of the test signal, and the test signal is successively transferred through the other chips (e.g., see Figure 5). By including the controller in only one of the chips, the size of the package is further reduced (see Specification at page 21, lines 18-23). The arguments herein for claim 10 apply as well to claim 11.

The final Office Action refers back to a previous Office Action of July 31, 2003. With respect to claim 11, the July 31 Office Action states that, "Brown et al. in view of Fehr disclose all subject matter claimed in claim 3 including Brown et al. teach a chip that includes a controller (TAP controller) for controlling an input/output interface of the test signal (see Fig. 4, "TAP controller"). *Also, Appellants note for the record that claim 11 depends from claim 10, and not from claim 3; The July 31 Office Action indicated that claim 11 included the subject matter of claim 3.*

Appellants agree that Brown teaches "a" chip in the standard-compliant board includes a controller. However, the claim is directed to, among other things, a semiconductor device having a plurality of chips, wherein "only the

one of said plurality of chips includes a controller for controlling an input/output interface of the test signal." Thus, Appellants submit that the rejection fails to establish *prima facie* obviousness for claim 11.

C. Rejection of claim 14 under 35 U.S.C. 103(a)

1. Argument Summary

The reasoning provided in support of the rejection of claim 14 under 35 U.S.C. § 103(a) as being unpatentable over *Brown* and *Fehr* fails to establish *prima facie* obviousness. Generally, the deficiency of the rejection is that Brown and Fehr, either alone or in combination, fail to show or suggest each and every claimed element.

Such a deficiency exists for the rejection of claim 14.

2. The rejection fails to establish *prima facie* obviousness of claim 14

Claim 14 is directed to a semiconductor device in which a plurality of chips are integrally sealed air-tight wherein, among other things,

"test commands/data input and output pins of a device is respectively connected to the test commands/data input and output pads of the chip of the first stage, and the relay output pad of the chip of the first stage is connected to a test commands/data input pad of a chip of a following stage, and a test commands/data output pad and a test commands/data input pad is serially and successively connected between chips of a preceding stage and a following

stage, and a test commands/data output pad of a chip of a last stage is connected to the relay input pad of the chip of the first stage so as to form a loop, and the output pads of the chip of the first stage for the signals to be used in the test is connected to input pads of the signals of the other chips, connection being performed via wires sealed with the plurality of chips."

Thus, the invention of claim 14 is directed to an integrally sealed package having a specific connection structure where the test commands/data input and output pins of the semiconductor device is respectively connected to the test commands/data input and output pads of the chip of the first stage and the test commands/data output pad of a chip of a last stage is connected to the relay input pad of the chip of the first stage so as to form a loop (see, for example, Figure 5).

The July 31 Office Action admits that Brown does not explicitly teach a single chip connected to the test signal input terminal and test result output terminal whereby the test signal is transferred to the other chips. Instead the Office Action appears to state that Brown suggests the claimed connection structure, and points out a section in Brown at column 4, lines 28-45. In particular, the Office Action states that Brown teaches mechanics of testing and capable of transferring data between on-chip logic side and the pin by which the chip is connected to the rest of the system "which Brown's techniques of transferring data is similar to the applicants method." Appellants believe that what the Office Action is implying is that because Brown discloses

techniques of transferring data, that Brown thereby suggests the claimed connection structure.

Claim 14 is directed to a semiconductor device, not a method of testing as implied in the Office Action by the statement "similar to applicants method." Also, claim 14 is directed to a connection structure between chips. Brown discloses data transfer capabilities defined by the Boundary Scan test standard for boundary scan cells within a standard-compliant chip (column 4, lines 28-36). As can be seen in Figure 1 of Brown, for example, a boundary scan cell is associated with each pin of the standard-compliant chip as well as the chip's "on-chip logic". Based on the discussion of data transfer capabilities, each cell can transfer data from the chip's "on-chip logic" to the cell's associated pin, from the chip's "on-chip logic" to a next cell, from a previous cell to itself, and from a previous cell to a next cell. Thus, the discussion of techniques of transferring data relied on in the Office Action actually pertains to data transfer within a chip.

Figure 2 of Brown shows a connection structure between chips on a standard-compliant circuit board (Figure 2 is also described in column 4, lines 3-27). It is clear from the figure that, for example, the first stage chip in the ring is connected the TDI edge connection, while the last stage chip is connected to the TDO edge connection.

Thus, Appellants submit that Brown fails to teach or suggest the specific claimed connection structure recited in claim 14, including at least wherein the

test commands/data input and output pins of a device is respectively connected to the test commands/data input and output pads of the chip of the first stage and a test commands/data output pad of a chip of a last stage is connected to the relay input pad of the chip of the first stage so as to form a loop.

The Office Action further admits that Brown does not disclose "in detail" the characteristics of the chip's air tight integral packaging. Appellants disagree that Brown even suggests a plurality of chips "integrally sealed".

Brown is directed to an architecture for intra-board and inter-board fault testing. In a background section, Brown provides basic information about Boundary Scan testing. In that section, Brown clearly teaches a plurality of chips arranged on a standard-compliant circuit board. For example, Brown states that, "IEEE Std 1149.1 - also referred to as "JTAG" – specifies testability standards for a circuit module made up of a number of interconnected ICs ("chips") mounted on a circuit board or its equivalent." In a further description of a standard-compliant board, Brown describes the connection structure shown in Figure 2 (at column 4, lines 3-27). Appellants submit that Brown's disclosed circuit board does not just omit details of chips being "integrally" sealed. In other words, there is no evidence to suggest that at least two of the chips of Brown's circuit board would be integrally sealed air-tight.

In any case, the Office Action goes on to rely on Fehr for teaching the claimed feature of air tight integral packaging. In particular, the Office Action

states that Fehr clearly teaches that IC chips are typically packaged in an air-tight environment. Furthermore, with respect to "integrally sealed" the Office Action states that, "it is clear that all chips contain different types of device such as transistors, capacitors and resistors. And encapsulating or sealing such a chip as in the prior art clearly implies the encapsulation of the chip with all the elements implying an "integrally sealed" structure."

It appears that the Office Action has misinterpreted the phrase "a plurality of chips are integrally sealed." The Office Action appears to imply that "integrally sealed" pertains to a single chip (based on the statement that a chip as well as its peripheral elements would be encapsulated, thus being "integrally sealed"). Based on this interpretation, the Office Action has admitted that neither Brown nor Fehr teach a plurality of chips integrally sealed. In any case, the claim does not recite that <u>each</u> chip is integrally sealed.

Appellants submit that claim 14 clearly refers to the level of "chip" and not components within the peripheral of a chip in its recitation, "a plurality of chips are integrally sealed air-tight". Therefore, Appellants submit that the rejection fails to establish *prima facie* obviousness at least with respect to this claimed element of claim 14.

Fehr is directed to a method for encapsulating IC packages having diamond substrate. However, Fehr does appear to mention that its encapsulated packages apply to dual in line designs (column 3, lines 50-51). Other than mentioning dual in line design, each of Fehr's disclosed

embodiments includes only a single IC die 43 encapsulated, and there is no disclosure of chips being connected for boundary scan testing. Therefore, Fehr does not at least make up for the deficiency of Brown of failing to teach or suggest a chip of the first stage being connected to both the test commands/data input and output pins of the semiconductor package, as well as the loop connection between the output pad of the chip of a last stage and the relay input pad of a chip of the first stage.

Thus, at least for the above reasons, Appellants submit that the rejection fails to establish *prima facie* obviousness.

D. Rejection of claim 13 under 35 U.S.C. 103(a)

1. Argument Summary

The reasoning provided in support of the rejection of claim 13 under 35 U.S.C. § 103(a) as being unpatentable over *Brown* and *Fehr* fails to establish *prima facie* obviousness. Generally, the deficiency of the rejection is that Brown and Fehr, either alone or in combination, fail to show or suggest each and every claimed element.

Such deficiencies exist for the rejection of claim 13.

2. The rejection fails to establish *prima facie* obviousness of claim 13

Claim 13 is directed to a semiconductor device in which a plurality of chips are integrally sealed air-tight wherein, among other things,

"a test commands/data input pin of a device is connected to the test commands/data input pad of a chip of a first stage, and the test commands/data output pad of each chip is connected to a corresponding output pins of the device and serially to the test commands/data input terminal of a chip of a following stage via the output pin of the device, and input pins of the device for the signals to be used in the test is connected to the corresponding input pins of the signals of each chip, connection being performed via wires sealed with the plurality of chips."

The July 31 Office Action points to Brown's Figure 2 as teaching serially connection to a test data input of a chip of a following stage. The final Office Action presents a further argument that Brown's figure 2 teaches that plurality of chips connected to each other and TDO pin of first chip's TAP connected directly to TDI pin of second chip; TDO pin of second chip connected directly to TDI pin of the third chip; and so forth and the TDO pin of the last chip goes to the external bus' TDO line (relying on col. 4, lines 12-16).

Claim 13, however, recites that the test commands/data output pad of each chip is connected to corresponding output pins of the device and serially to the test commands/data input pad of a chip of a following stage via the output pin of the device. Figure 2 of Brown does not show at least a connection between an output pin of the device and a test commands/data input pad of a chip. In the invention of claim 13, by connecting the test commands/data input pad of a chip of a following stage to the output pin of the device, the

output pin of the device serves as a connection medium and avoids a direct connection between chips, further reducing package size (e.g., see Figure 4).

The Office Action further admits that Brown does not disclose "in detail" the characteristics of the chip's air tight integral packaging. Appellants disagree that Brown even suggests a plurality of chips "integrally sealed".

Brown is directed to an architecture for intra-board and inter-board fault testing. In a background section, Brown provides basic information about Boundary Scan testing. In that section, Brown clearly teaches a plurality of chips arranged on a standard-compliant circuit board. For example, Brown states that, "IEEE Std 1149.1 - also referred to as "JTAG" – specifies testability standards for a circuit module made up of a number of interconnected ICs ("chips") mounted on a circuit board or its equivalent." In a further description of a standard-compliant board, Brown describes the connection structure shown in Figure 2 (at column 4, lines 3-27). Appellants submit that Brown's disclosed circuit board does not just omit details of chips being "integrally" sealed. In other words, there is no evidence to suggest that at least two of the chips of Brown's circuit board would be integrally sealed air-tight.

In any case, the Office Action goes on to rely on Fehr for teaching the claimed feature of air tight integral packaging. In particular, the Office Action states that Fehr clearly teaches that IC chips are typically packaged in an air-tight environment. Furthermore, with respect to "integrally sealed" the Office Action states that, "it is clear that all chips contain different types of device

such as transistors, capacitors and resistors. And encapsulating or sealing such a chip as in the prior art clearly implies the encapsulation of the chip with all the elements implying an "integrally sealed" structure."

It appears that the Office Action has misinterpreted the phrase "a plurality of chips are integrally sealed." The Office Action appears to imply that "integrally sealed" pertains to a single chip (based on the statement that a chip as well as its peripheral elements would be encapsulated, thus being "integrally sealed"). Based on this interpretation, the Office Action has admitted that neither Brown nor Fehr teach a plurality of chips integrally sealed. In any case, the claim does not recite that each chip is integrally sealed.

Appellants submit that claim 13 clearly refers to the level of "chip" and not components within the peripheral of a chip in its recitation, "a plurality of chips are integrally sealed air-tight". Therefore, Appellants submit that the rejection fails to establish *prima facie* obviousness at least with respect to this claimed element of claim 13.

Fehr is directed to a method for encapsulating IC packages having diamond substrate. However, Fehr does appear to mention that its encapsulated packages apply to dual in line designs (column 3, lines 50-51). Other than mentioning dual in line design, each of Fehr's disclosed embodiments includes only a single IC die 43 encapsulated, and there is no disclosure of chips being connected for boundary scan testing. Therefore, Fehr does not at least make up for the deficiency of Brown of failing to teach or

suggest that the test commands/data output pad of each chip is connected to corresponding output pins of the device and serially to the test commands/data input pad of a chip of a following stage via the output pin of the device.

Thus, at least for this additional reason, Appellants submit that the rejection fails to establish *prima facie* obviousness.

E. Rejection of claims 3, 7, and 10 under 35 U.S.C. 103(a)

1. Argument Summary

The reasoning provided in support of the rejection of claims 3, 7, and 10 under 35 U.S.C. § 103(a) as being unpatentable over *Brown* and *Fehr* fails to establish *prima facie* obviousness. Generally, the deficiency of the rejection is that Brown and Fehr, either alone or in combination, fail to show or suggest each and every claimed element.

Such a deficiency exists for the rejection of claims 3, 7, and 10.

2. The rejection fails to establish *prima facie* obviousness of claims 3, 7, and 10

Claim 3 is directed to a semiconductor device in which a plurality of chips are integrally sealed air-tight wherein, among other things,

"only one of said plurality of chips being connected to said test signal input terminal, to said test result output terminal, and to said control signal input terminals" and "the test signal being inputted to the one of said plurality

of chips and successively transferred through the other chips, and after being inputted again into the one of said plurality of chips, outputted as the test result outside."

Thus, the invention of claim 3 is directed to an integrally sealed package having a specific connection structure where only one of the plurality of chips is connected to the test signal input terminal, to the test result output terminal, and to said control signal input terminals (see, for example, Figure 5). The claim defines the test signal input terminal as a terminal for receiving an externally supplied test signal. The test result output terminal is a terminal for outputting a test result of the plurality of chips to outside.

The July 31 Office Action admits that Brown does not explicitly teach a single chip connected to the test signal input terminal and test result output terminal whereby the test signal is transferred to the other chips. Instead the Office Action appears to state that Brown suggests the claimed connection structure, and points out a section in Brown at column 4, lines 28-45. In particular, the Office Action states that Brown teaches mechanics of testing and capable of transferring data between on-chip logic side and the pin by which the chip is connected to the rest of the system "which Brown's techniques of transferring data is similar to the applicants method." Appellants believe that what the Office Action is implying is that because Brown discloses techniques of transferring data, that Brown thereby suggests the claimed connection structure.

Claim 3 is directed to a semiconductor device, not a method of testing as implied in the Office Action by the statement "similar to applicants method." Also, claim 3 is directed to a connection structure between chips. On the other hand, Brown discloses data transfer capabilities defined by the Boundary Scan test standard for boundary scan cells within a standard-compliant chip (column 4, lines 28-36). As can be seen in Figure 1 of Brown, for example, a boundary scan cell is associated with each pin of the standard-compliant chip as well as the chip's "on-chip logic". Based on the discussion of data transfer techniques, each cell can transfer data from the chip's "on-chip logic" to the cell's associated pin, from the chip's "on-chip logic" to a next cell, from a previous cell to itself, and from a previous cell to a next cell. Thus, the discussion of techniques for transferring data relied on in the Office Action actually pertains to data transfer within a chip.

Figure 2 of Brown shows a connection structure between chips on a standard-compliant circuit board (Figure 2 is also described in column 4, lines 3-27). It is clear from the figure that, for example, the first stage chip in the ring is connected the TDI edge connection, while the last stage chip is connected to the TDO edge connection.

Thus, Appellants submit that Brown fails to teach or suggest the specific claimed connection structure recited in claim 3, including at least wherein only one of the plurality of chips is connected to the test signal input terminal, to the test result output terminal, and to the control signal input terminals.

The Office Action further admits that Brown does not disclose "in detail" the characteristics of the chip's air tight integral packaging. Appellants disagree that Brown even suggests a plurality of chips "integrally sealed".

Brown is directed to an architecture for intra-board and inter-board fault testing. In a background section, Brown provides basic information about Boundary Scan testing. In that section, Brown clearly teaches a plurality of chips arranged on a standard-compliant circuit board. For example, Brown states that, "IEEE Std 1149.1 - also referred to as "JTAG" – specifies testability standards for a circuit module made up of a number of interconnected ICs ("chips") mounted on a circuit board or its equivalent." In a further description of a standard-compliant board, Brown describes the connection structure shown in Figure 2 (at column 4, lines 3-27). Appellants submit that Brown's disclosed circuit board does not just omit details of chips being "integrally" sealed. In other words, there is no evidence to suggest that at least two of the chips of Brown's circuit board would be integrally sealed air-tight.

In any case, the Office Action goes on to rely on Fehr for teaching the claimed feature of air tight integral packaging. In particular, the Office Action states that Fehr clearly teaches that IC chips are typically packaged in an air-tight environment. Furthermore, with respect to "integrally sealed" the Office Action states that, "it is clear that all chips contain different types of device such as transistors, capacitors and resistors. And encapsulating or sealing

such a chip as in the prior art clearly implies the encapsulation of the chip with all the elements implying an "integrally sealed" structure."

It appears that the Office Action has misinterpreted the phrase "a plurality of chips are integrally sealed." The Office Action appears to imply that "integrally sealed" pertains to a single chip (based on the statement that a chip as well as its peripheral elements would be encapsulated, thus being "integrally sealed"). Based on this interpretation, the Office Action has admitted that neither Brown nor Fehr teach a plurality of chips integrally sealed. In any case, the claim does not recite that each chip is integrally sealed.

Appellants submit that claim 3 clearly refers to the level of "chip" and not components within the peripheral of a chip in its recitation, "a plurality of chips, which are integrally sealed air-tight". Therefore, Appellants submit that the rejection fails to establish *prima facie* obviousness at least with respect to this claimed element of claim 3.

Fehr is directed to a method for encapsulating IC packages having diamond substrate. However, Fehr does appear to mention that its encapsulated packages apply to dual in line designs (column 3, lines 50-51). Other than mentioning dual in line design, each of Fehr's disclosed embodiments includes only a single IC die 43 encapsulated, and there is no disclosure of chips being connected for boundary scan testing. Therefore, Fehr does not at least make up for the deficiency of Brown of failing to teach or suggest one of the plurality of chips being connected such that only one of the

plurality of chips is connected to the test signal input terminal, to the test result output terminal, and to the control signal input terminals.

Claim 7, comparable to the above for claim 3, recites test commands/data input and output terminal of the device being respectively connected to the test commands/data input and output terminals of the chip of the first stage. In other words, the chip of the first stage is recited as being connected to both the test commands/data input terminal and test commands/data output terminal of the device.

Claim 10, also comparable to the above for claim 3, recites only one of the plurality of chips being connected to the test signal input pin, to the test result output pin, and to the test control signal pins.

Thus, at least for the above reasons, Appellants submit that the rejection fails to establish *prima facie* obviousness for claims 3, 7, and 10.

F. Rejection of claims 2, 6, and 9 under 35 U.S.C. 103(a)

1. Argument Summary

The reasoning provided in support of the rejection of claims 2, 6, and 9 under 35 U.S.C. § 103(a) as being unpatentable over *Brown* and *Fehr* fails to establish *prima facie* obviousness. Generally, the deficiency of the rejection is that Brown and Fehr, either alone or in combination, fail to show or suggest each and every claimed element.

Such a deficiency exists for the rejection of claims 2, 6, and 9.

2. The rejection fails to establish *prima facie* obviousness of claims 2, 6, and 9

Claim 2 is directed to a semiconductor device in which a plurality of chips are integrally sealed air-tight wherein, among other things, "wherein said plurality of chips are connected to each other via said test result output terminal." Claim 2 defines test result output terminal as a terminal for outputting a test result of the plurality of chips to outside.

The July 31 Office Action states that Brown teaches a plurality of chips connected to each other through test result output terminal in a section at column 4, lines 3-27. That section describes the example standard-compliant circuit board shown in Figure 2. Brown's figure 2 is described as showing a plurality of chips connected to each other such that the TDO pin of first chip's TAP is connected directly to TDI pin of second chip; the TDO pin of the second chip connected directly to TDI pin of the third chip; and so forth, and the TDO pin of the last chip goes to the external bus' TDO line.

Claim 2, however, recites that a plurality of chips are connected to each other via the test result output terminal. Figure 2 of Brown does not appear to show at least two chips connected by way of the output terminal of the circuit board. In the invention of claim 2, by connecting a plurality of chips via the test result output terminal, the output terminal of the device serves as a connection medium and avoids a direct connection between chips, further reducing package size (e.g., see Figure 4).

The Office Action further admits that Brown does not disclose "in detail" the characteristics of the chip's air tight integral packaging. Appellants disagree that Brown even suggests a plurality of chips "integrally sealed".

Brown is directed to an architecture for intra-board and inter-board fault testing. In a background section, Brown provides basic information about Boundary Scan testing. In that section, Brown clearly teaches a plurality of chips arranged on a standard-compliant circuit board. For example, Brown states that, "IEEE Std 1149.1 - also referred to as "JTAG" – specifies testability standards for a circuit module made up of a number of interconnected ICs ("chips") mounted on a circuit board or its equivalent." In a further description of a standard-compliant board, Brown describes the connection structure shown in Figure 2 (at column 4, lines 3-27). Appellants submit that Brown's disclosed circuit board does not just omit details of chips being "integrally" sealed. In other words, there is no evidence to suggest that at least two of the chips of Brown's circuit board would be integrally sealed air-tight.

In any case, the Office Action goes on to rely on Fehr for teaching the claimed feature of air tight integral packaging. In particular, the Office Action states that Fehr clearly teaches that IC chips are typically packaged in an air-tight environment. Furthermore, with respect to "integrally sealed" the Office Action states that, "it is clear that all chips contain different types of device such as transistors, capacitors and resistors. And encapsulating or sealing

such a chip as in the prior art clearly implies the encapsulation of the chip with all the elements implying an "integrally sealed" structure."

It appears that the Office Action has misinterpreted the phrase "a plurality of chips are integrally sealed." The Office Action appears to imply that "integrally sealed" pertains to a single chip (based on the statement that a chip as well as its peripheral elements would be encapsulated, thus being "integrally sealed"). Based on this interpretation, the Office Action has admitted that neither Brown nor Fehr teach a plurality of chips integrally sealed. In any case, the claim does not recite that each chip is integrally sealed.

Appellants submit that claim 2 clearly refers to the level of "chip" and not components within the peripheral of a chip in its recitation, "a plurality of chips, which are integrally sealed air-tight". Therefore, Appellants submit that the rejection fails to establish *prima facie* obviousness at least with respect to this claimed element of claim 2.

Fehr is directed to a method for encapsulating IC packages having diamond substrate. However, Fehr does appear to mention that its encapsulated packages apply to dual in line designs (column 3, lines 50-51). Other than mentioning dual in line design, each of Fehr's disclosed embodiments includes only a single IC die 43 encapsulated, and there is no disclosure of chips being connected for boundary scan testing. Therefore, Fehr does not at least make up for the deficiency of Brown of failing to teach or suggest one of the plurality of chips being connected to both the test

commands/data input and output pins of the semiconductor package, as well as the loop connection between the output pad of the chip of a last stage and the relay input pad of a chip of the first stage.

Claim 6, comparable to claim 2, recites the test commands/data output terminal of a chip being connected to a corresponding output terminal of the device and serially to the test commands/data input terminal of a chip of a following stage via the output terminal of the device.

Claim 9, comparable to claim 2, recites wherein the plurality of chips are connected to each other via the test result output pin. The test result output pin is defined as a pin for outputting a test result of the plurality of chips to outside.

Thus, at least for these reasons, Appellants submit that the rejection fails to establish *prima facie* obviousness for claims 2, 6, and 10.

G. Rejection of claim 15 under 35 U.S.C. 103(a)

1. Argument Summary

The reasoning provided in support of the rejection of claim 15 under 35 U.S.C. § 103(a) as being unpatentable over *Brown* and *Fehr* fails to establish *prima facie* obviousness. Generally, the deficiency of the rejection is that it fails to particularly point out evidence of the additional feature recited in the claim

and Brown fails to show or suggest that feature. Such deficiencies exist for the rejection of claim 15.

2. The rejection fails to establish *prima facie* obviousness of claim 15

Claim 15 is directed to the invention of claim 2 as well as wherein the plurality of chips are stacked, such that at least two of the chips substantially overlap. Thus, the invention of claim 15 includes, among other things, a plurality of chips which are integrally sealed air-tight and that are stacked such that they substantially overlap (an example of the invention of claim 15 is shown in Figure 2). The arguments above for claim 2 apply as well to claim 15.

The final Office Action refers back to a previous Office Action of July 31, 2003. Claim 15 had been added in an Amendment filed June 27, 2003. With respect to claim 15, the July 31 Office Action states that, "Brown et al. in view of Fehr disclose all subject matter claimed in claim 1 including Brown et al. teach plurality of chips connected to each other through test output terminal (see col. 4, lines 3-27)." The rejection is deficient in that it does not point out where the claimed integrally sealed stacked plurality of chips is taught or suggested in either of the references.

Appellants submit that the rejection fails to particularly point out where all claim limitations are taught or suggested by the prior art and thus fails to establish *prima facie* obviousness.

Further, even if Brown can be generally relied on, Appellants submit that Brown fails to teach or suggest at least the element recited in dependent claim 15. The section of Brown relied on in the rejection describes a "standard-compliant board" in accordance with IEEE Std 1149.1, the Boundary-Scan testing standard. Figure 2 illustrates an example standard-compliant board. The reason for the test standard was to ensure uniformity in test-architecture and a test protocol (col. 3, lines 28-37). Basically, the standard, as shown in Figure 2, pertains to a test architecture consisting of circuit boards (standard-compliant boards or modules) having standard-compliant devices connected together into test rings by standard-compliant local test buses accessible at the edge connectors (column 3, lines 40-47). In other words, chips mounted in a test-ring on the circuit board are connected in a daisy-chain (column 4, lines 19-22). The circuit board and daisy-chained connected chips shown in Figure 2 is disclosed as prior art. Brown discloses an invention that expands the fault-testing based on the testing standard to testing of logic circuits made up of multiple individual modules, each of which is compliant with the Boundary Scan test standard (column 12, lines 47-50).

Thus, Appellants submit that Brown fails to teach or suggest at least the feature of a plurality of chips stacked, such that at least two of the chips substantially overlap.

H. Rejection of claim 16 under 35 U.S.C. 103(a)

1. Argument Summary

The reasoning provided in support of the rejection of claim 16 under 35 U.S.C. § 103(a) as being unpatentable over *Brown* and *Fehr* fails to establish *prima facie* obviousness. Generally, the deficiency of the rejection is that it fails to particularly point out evidence of the additional feature recited in the claim and Brown fails to show or suggest that feature. Such deficiencies exist for the rejection of claim 16.

2. The rejection fails to establish *prima facie* obviousness of claim 16

Claim 16 is directed to the invention of claim 3 as well as wherein the plurality of chips are stacked, such that at least two of the chips are stuck on front and back surfaces of a substrate, respectively. Thus, the invention of claim 16 includes, among other things, a plurality of chips which are integrally sealed air-tight and that are stacked on opposite surfaces of a substrate (an example of the invention of claim 16 is shown in Figure 4). The arguments above for claim 3 apply as well to claim 16.

The final Office Action refers back to a previous Office Action of July 31, 2003. Claim 16 had been added in an Amendment filed June 27, 2003. With respect to claim 16, the July 31 Office Action states that, "Brown et al. in view of Fehr disclose all subject matter claimed in claim 3 including Brown et al. teach a chip that includes a controller (TAP controller) for controlling an input/output interface of the test signal (see Fig. 4, "TAP controller"). The

rejection is deficient in that it does not point out where the claimed integrally sealed stacked plurality of chips is taught or suggested in either of the references.

Appellants submit that because the claimed element of claim 16 is not addressed in any Office Action, that the rejection fails to establish *prima facie* obviousness.

Further, even if Brown can be generally relied on, Appellants submit that Brown fails to teach or suggest at least the element recited in dependent claim 16. The section of Brown relied on in the rejection pertains to a standard-compliant board loaded with two-standard-compliant chips (e.g., Figure 4; column 5, lines 62-66). Brown discloses an invention that expands the fault-testing based on the testing standard (e.g., that shown in Figure 4) to testing of logic circuits made up of multiple individual modules, each of which is compliant with the Boundary Scan test standard (column 12, lines 47-50).

Thus, Appellants submit that Brown fails to teach or suggest at least the claimed plurality of chips stacked, such that at least two of the chips are stuck on front and back surfaces of a substrate.

X. CONCLUSION

For the reasons specifically set forth above, the outstanding rejections set forth in the Final Office Action should be reversed.

Respectfully submitted,

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APPENDIX OF CLAIMS

1. (canceled)

2. (previously presented) A semiconductor device, comprising:

a plurality of chips, which are integrally sealed air-tight;

a test signal input terminal for receiving an externally supplied test signal;

a test result output terminal for outputting a test result of said plurality of chips to outside; and

control signal input terminals for receiving externally supplied test control signals,

the test signal inputted from said test signal input terminal being successively transferred through said plurality of chips, and

the test control signals inputted from said control signal input terminals being individually supplied to each of said plurality of chips,

wherein said plurality of chips are connected to each other via said test result output terminal.

3. (previously presented) A semiconductor device, comprising:

a plurality of chips, which are integrally sealed air-tight;

a test signal input terminal for receiving an externally supplied test signal;

a test result output terminal for outputting a test result of said plurality of chips to outside; and

control signal input terminals for receiving externally supplied test control signals,

only one of said plurality of chips being connected to said test signal input terminal, to said test result output terminal, and to said control signal input terminals,

the test signal being inputted to the one of said plurality of chips and successively transferred through the other chips, and after being inputted again into the one of said plurality of chips, outputted as the test result outside, and

the test control signals being individually supplied from the one of said plurality of chips to each of the other chips.

4. (Original) The semiconductor device as set forth in claim 3, wherein only the one of said plurality of chips includes a controller for controlling an input/output interface of the test signal.

5. (canceled)

6. (previously presented) A semiconductor device in which a plurality of chips are integrally sealed air-tight, comprising:

a test register provided between a core logic and each of input and output terminals of each chip; and

a control circuit for controlling said test register for testing the chip, test commands/data input and output terminals connected to said control circuit, and input terminals of signals, connected to said control circuit, to be used in the test, which are all mounted on each chip,

a test commands/data input terminal of a device being connected to the test commands/data input terminal of a chip of a first stage, and the test commands/data output terminal of a chip being connected to a corresponding output terminal of the device and serially to the test commands/data input terminal of a chip of a following stage via the output terminal of the device, and input terminals of the device for the signals to be used in the test being connected to the corresponding input terminals of the signals of each chip.

7. (previously presented) A semiconductor device in which a plurality of chips are integrally sealed air-tight, comprising:

a test register provided between a core logic and each of input and output terminals of each chip; and

a control circuit for controlling the test register for testing the chip, test commands/data relay input and output terminals connected to said control circuit, and output terminals of signals to be used in the test outputted from the control circuit, which are all mounted on a chip of a first stage,

test commands/data input and output terminals of a device being respectively connected to the test commands/data input and output terminals of the chip of the first stage, and the relay output terminal of the chip of the first stage being connected to a test commands/data input terminal of a chip of a following stage, and a test commands/data output terminal and a test commands/data input terminal being serially and successively connected between chips of a preceding stage and a following stage, and a test commands/data output terminal of a chip of a last stage being connected to the relay input terminal of the chip of the first stage so as to form a loop, and the output terminals of the chip of the first stage for the signals to be used in the test being connected to input terminals of the signals of the other chips.

8. (canceled)

9. (previously presented) A semiconductor device, comprising:

a plurality of chips, which are integrally sealed air-tight;

a test signal input pin for receiving an externally supplied test signal;

a test result output pin for outputting a test result of said plurality of chips to outside; and

control signal input pins for receiving externally supplied test control signals,

the test signal inputted from said test signal input pin being successively transferred through said plurality of chips connected with each other by wires sealed with said plurality of chips, and

the test control signals inputted from said control signal input pins being individually supplied to each of said plurality of chips via wires sealed with the plurality of chips,

wherein said plurality of chips are connected to each other via said test result output pin.

10. (previously presented) A semiconductor device, comprising:

a plurality of chips, which are integrally sealed air-tight;

a test signal input pin for receiving an externally supplied test signal;

a test output pin for outputting a test result of said plurality of chips to outside; and

control signal input pins for receiving externally supplied test control signals,

only one of said plurality of chips being connected to said test signal input pin, to said test result output pin, and to said control signal input pins,

the test signal being inputted to the one of said plurality of chips and successively transferred through the other chips so connected to each other by wires sealed with the plurality of chips, and after being inputted again into the one of said plurality of chips, outputted as the test result to outside, and

the test control signals being individually supplied from the one of said plurality of chips to each of the other chips via wires sealed with the plurality of chips.

11. (Previously Presented) The semiconductor device as set forth in claim 10, wherein only the one of said plurality of chips includes a controller for controlling an input/output interface of the test signal.

12. (canceled)

13. (currently amended) A semiconductor device in which a plurality of chips are integrally sealed air-tight, comprising:

a test register provided between a core logic and each of input and output terminals of each chip; and

a control circuit for controlling said test register for testing the chip, test commands/data input and output pads connected to said control circuit, and input pads of signals, connected to said control circuit, to be used in the test, which are all mounted on each chip, wherein

a test commands/data input pin of a device is connected to the test commands/data input pad of a chip of a first stage, and the test commands/data output pad of each chip is connected to a corresponding output pins of the device and serially to the test commands/data input

terminal of a chip of a following stage via one of the output pins of the device, and input pins of the device for the signals to be used in the test is connected to the corresponding input pins of the signals of each chip, connection being performed via wires sealed with the plurality of chips.

14. (previously presented). A semiconductor device in which a plurality of chips are integrally sealed air-tight, comprising:

a test register provided between a core logic and each of input and output terminals of each chip; and

a control circuit for controlling the test register for testing the chip, test commands/data relay input and output pads connected to said control circuit, and output pads of signals to be used in the test outputted from the control circuit, which are all mounted on a chip of a first stage, wherein

test commands/data input and output pins of a device is respectively connected to the test commands/data input and output pads of the chip of the first stage, and the relay output pad of the chip of the first stage is connected to a test commands/data input pad of a chip of a following stage, and a test commands/data output pad and a test commands/data input pad is serially and successively connected between chips of a preceding stage and a following stage, and a test commands/data output pad of a chip of a last stage is connected to the relay input pad of the chip of the first stage so as to form a loop, and the output pads of the chip of the first stage for the signals to be

used in the test is connected to input pads of the signals of the other chips, connection being performed via wires sealed with the plurality of chips.

15. (previously presented) The semiconductor device as set forth in claim 2, wherein said plurality of chips are stacked, such that at least two of the chips substantially overlap.

16. (previously presented) The semiconductor device as set forth in claim 3, wherein said plurality of chips are stacked, such that at least two of the chips are stuck on front and back surfaces of a substrate, respectively.